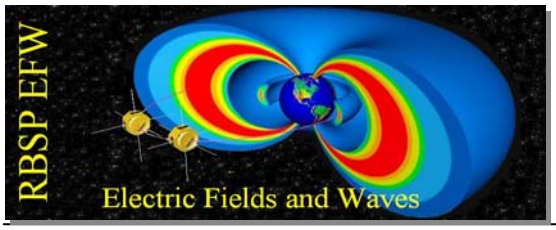

RBSP EFW
Instrument Data Processing Unit (IDPU)
Backplane Specification

RBSP_EFW_BPL_001P_Specification.doc
3/18/2010

Michael Ludlam
2010.03.18
11:15:38 -07'00'

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2010.04.05
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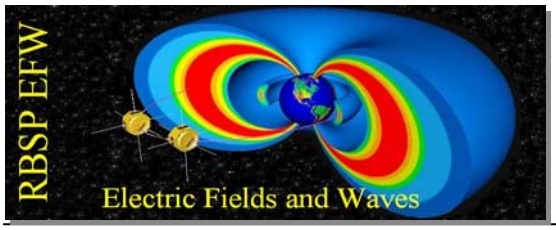

Document Revision Record

Rev.	Date	Description of Change	Approved By
A	9/21/07	Preliminary Draft	-
B	1/4/08	Update	
C	5/9/08	First Full Release	
D		Deleted BEB Relays, Added DAC Trip, Aft Boom shutdown pin, corrected DFB-DCB TLM description	
E	7/28/08	Deleted EMF_MAG_GAIN_STATE renamed to DIG_SPARE0	
F	8/6/08	AFT_SHUTDOWN removed from backplane, 5.5V supplies replaced with 5V. Corrected EMF_MAG_GAIN Section.	
G	8/808	Removed the DAC Trip Signals from the BEB interface	
H	11/21/08	Added BEB_DACCS pin to backplane connector	
I	11/26/08	Minor changes to correct errors and include missing LVPS pins to backplane.	
J	12/10/08	Modifications to timing diagrams and other small edits.	
K	12/15/08	Updates to add redundancy to the DIN96	
L	6/9/09	Corrected part number for LVPS connector Changed BEB, DFB, DCB connectors for KA98 Updated LVPS Clock frequency to 799kHz	
M	7/31/09	Added Analog Spares	
P	3/18/10	Removed reference to DIN96 and added Hypertronics keying	

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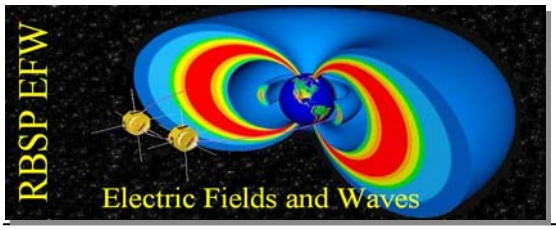
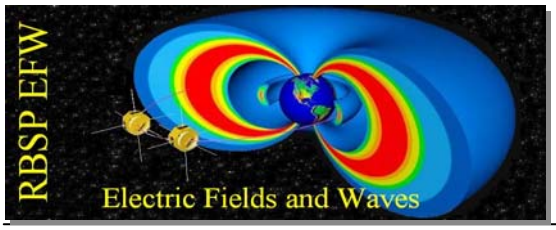


TBDs

Identifier	Description

Reference Documents

Document Ref	Description
RBSP_EFW_SYS_001	EFW System Requirements
RBSP_EFW_DCB_003	DCB Specification
RBSP_EFW_DFB_001	DFB Specification
RBSP_EFW_BEB_001	BEB Specification
RBSP_EFW_LVPS_001	LVPS and PCB Specification



1 Overview

The RBSP EFW IDPU backplane provides the essential communications and power services between the Data Controller Board (DCB), Digital Fields Board (DFB), the Boom Electronics Board (BEB), the Power Controller Board (PCB), and the Low Voltage Power Supply (LVPS) inside the Instrument Data Processor Unit (IDPU) for the EFW instrument on RBSP.

2 Requirements

2.1 Data Controller Board (DCB)

Power: The DCB is always powered when the IDPU is powered. The DCB requires the following voltages: +1.8VD, +3.6VD, 5VD, +5VA, -5VA, +10VA, -10VA all provided by the LVPS.

Commands: The DCB interacts with the other cards with serial interfaces as described below. The DCB is the master on the backplane i.e. it sends all the commands and receives none.

Telemetry: The DCB receives telemetry on either of two separate pins on the backplane from the DFB board. The DCB sends no telemetry on the backplane.

Analog Housekeeping: The DCB contains the A/D converter for sampling housekeeping analogs. It receives analog inputs on the backplane from the PCB/LVPS and BEB boards.

2.2 Digital Fields Board (DFB)

Power: The DFB is always powered when the IDPU is powered. The DFB requires the following voltages: +1.8VD, +3.6VD, 5VD, +5VA, -5VA, +10VA, -10VA all provided by the LVPS.

Commands: The DFB requires a command interface that can configure the board after each turn-on. During collection mode transitions of the IDPU, the Flight Software (FSW) will send a series of commands to the DFB. The command interface is further detailed below.

Telemetry: The DFB sends digital data to the DCB on either of two pins and should meet EFW requirement to using an Address/Data scheme on a serial transfer as described below.

Housekeeping: The DFB requires no analog housekeeping. It returns housekeeping via a separate DataID as detailed in the DFB Specification (RBSP_EFW_DFB_001).

2.3 Boom Electronics Board (BEB)

Power: The BEB is always powered when the IDPU is powered. The BEB requires the following voltages: 5VD, +10VA, -10VA, +225VA, -225VA and six separate +15VF, -15VF and FGND for each boom system.

Commands: The BEB requires a command interface to configure the board after each turn-on. On failure of the DCB, after a power cycle the BEB will default to a configuration specified in RBSP_EFW_BEB_001 (BEB board specification). The command interface is detailed below.

Telemetry: The BEB produces no telemetry.

Housekeeping: The BEB will use a separate analog housekeeping line to multiplex about 20 voltages to the DCB.

2.4 Low Voltage Power Supply (LVPS) & Power Control Board (PCB)

Power: The LVPS provides the power to the IDPU boards via the PCB. The LVPS and PCB are always powered when the IDPU is powered on. It also switches power to drive the actuation services. The LVPS and PCB circuits share a single board.

Commands: The PCB circuitry requires a command interface to turn on/off actuation services and address its' multiplexer. PCB also provides control for the LVPS switches on the primary power side.

Telemetry: The PCB produces no telemetry.

Analog Housekeeping: The PCB has a number of voltages (currents, etc). These are fed through a mux addressed by commands to the PCB logic, and fed up the backplane on a separate analog housekeeping line to the DCB for A/D conversion.

3 Command & Telemetry Signal Interfaces

There are three separate communication protocols between the DCB and individual boards. The DCB-DFB interface uses the SSL/UCB standard CDI (Command & Data Interface), a serial protocol, synchronized to a 2^{23}Hz clock provided by the DCB. The DCB-PCB/LVPS interface is a simpler 3 line (command, clock and strobe) interface whereas the DCB-BEB interface is a series of lines that directly control circuitry on the BEB. More details on each interface are found below.

3.1 Common Serial Interface Circuit

Although each interface is slightly different they share a common circuit as shown in Figure 1 below. Series termination is provided to slow clock edges and reduce ringing. It is expected that the maximum transmission length is about 8 inches. The resistors at the receiving end protect the gate input and pull it to an inactive level when disconnected. The driver may be any 54AC gate, but the 54AC14 is a standard way to buffer the signals and provide hysteresis and is therefore the recommended first circuit device.

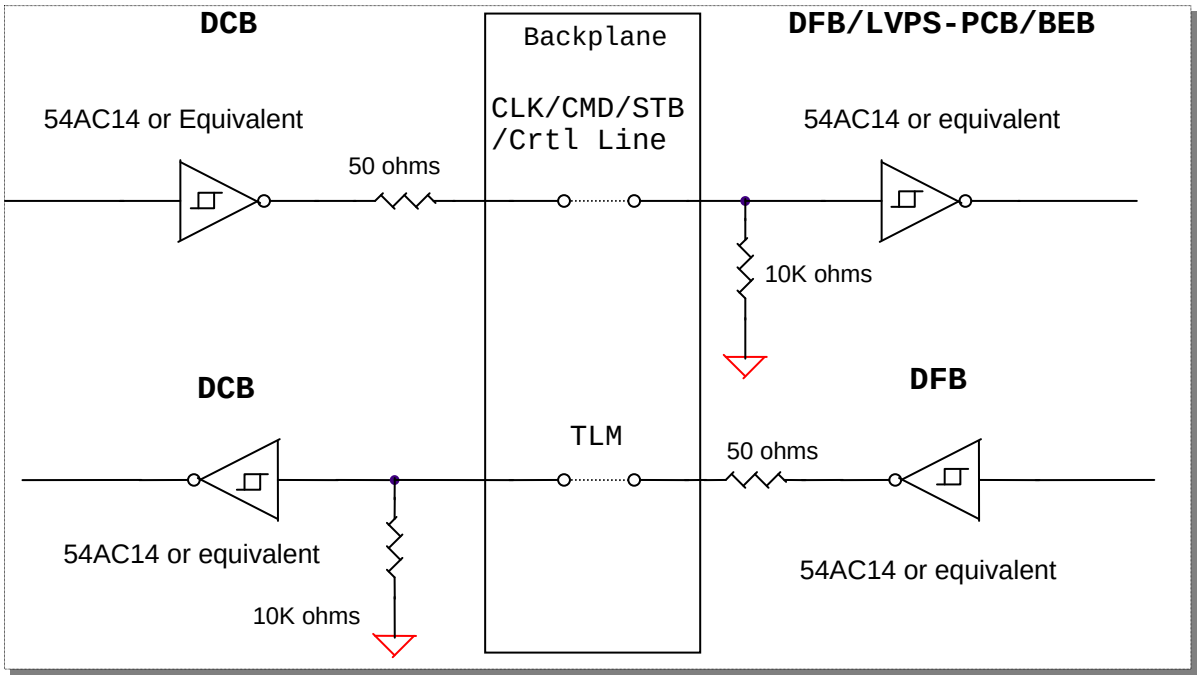


Figure 1 - Serial Interface Circuit

3.2 DFB – DCB Interface

The DFB-DCB interface is all at 3.3V.

3.2.1 Commands

Commands from the DCB to the DFB shall be formatted into 24 bit data words (8 bits of identification and 16 bits of information), and passed serially on the command signal "CMD". A parity bit follows the 24-bit data word. Start and stop bits shall be used to synchronize transmissions. A list of the 8 bit identifiers can be found in the DFB specification document (RBSP_EFW_DFB_001). Figure 2 shows the command interface timing. Note all signal polarities are as measured on the backplane.

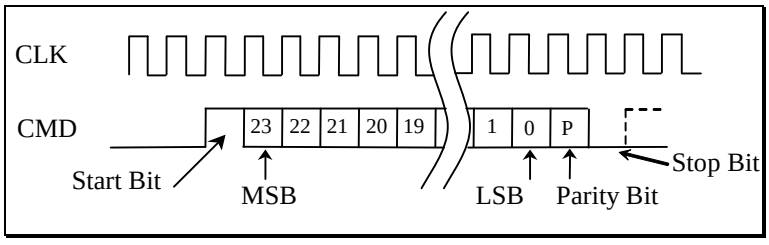


Figure 2 - Serial Command Timing

The receiving circuit should clock in the data bits on the falling edge of CLK (to avoid a race between the CMD and CLK signals). The system synchronizes by finding the first non-zero bit (the START bit), and verifies synchronization by the presence of a zero-value STOP bit. After a reset or loss of synchronization,

the receiving system should look for 25 consecutive zero-level bits before starting to look for a start bit to avoid incorrect interpretation of a transfer in progress. The 24 bits are sent MSB first. The parity is odd and includes the 24 command bits but not the start bit, so that a command with all 24 bits zero would have the parity bit on. Commands can start on any rising edge of CLK, and any number of idle bit periods can occur between commands. It is expected that the DFB will reject commands with bad parity or framing (no stop bit), and optionally report an interface error in their telemetry stream. No automatic commands retries will be attempted.

3.2.2 EMFISIS Magnetometer Gain

The EMFISIS instrument provides magnetometer gain information to the DCB board via the spacecraft interface. This is now transmitted to the DFB via a command; see the command and telemetry specification document for details.

3.2.3 Telemetry

Data from the instrument shall be formatted into blocks of 16 bit words transferred serially over the data signal "TLM0" or “TLM1” sent as 27 bits over a 32 bit period. Start gaps between messages and words synchronize transmissions. Following the start bit there is an 8 bit of message ID followed by the 16 bits of data. The stop bit and parity bit follow this. The parity is odd. The two telemetry streams are synchronous but 16 bits out of phase.

The DFB shall shift the next bit of the message out on the rising edge of CLK. The bit will be sampled by the DCB on the next rising edge of CLK. Telemetry is synchronized by having messages preceded by at least 27 bits of zero. The DCB shall synchronize to the first non-zero bit as the START bit of the first word of the message. No other handshaking is planned. Transfers are coded via the 8-bit Applications Identifiers (ApIDs) and these are detailed in the DFB specification document (RBSP_EFW_DFB_001). Figure 3 shows the telemetry interface timing. Note all signal polarities are as measured on the backplane.

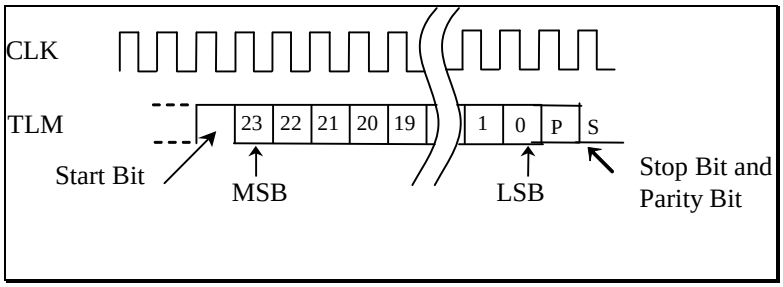


Figure 3 - Serial Telemetry Timing

3.2.4 Time Synchronization

The backplane provides two generic timing pulses, separately buffered: DCB8MHZ (which also serves as CLK for the DFB, used for timing CMD and TLM data) and DCB1HZ (the one second synch). These clocks are based on the free running oscillator on the DCB board. The spacecraft provides a separate 1HZ for time tagging packets but this is independent to the DFB_1HZ tick. CLK8MHZ is a 2^{23} Hz and CLK1HZ is a 1Hz clock. These clocks are synchronous; there are always 2^{23} CLK8MHZ clocks per CLK1HZ clock pulse. The timing of these clocks is shown below in figure 4.

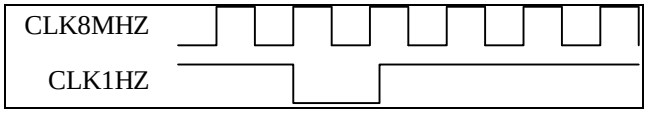


Figure 4 - Clock Timing

Note that CLK1HZ is always asserted slightly after the rising edge of CLK8MHZ. If CLK1HZ is used as a synchronous input, the DFB should clock CLK1HZ at the falling edge of CLK8MHZ (in order to avoid potential hold-time hazards).

3.3 BEB – DCB Interface

The BEB-DCB interface is all 5V logic.

3.3.1 Commands

The BEB board receives control line signals from the DCB on 12 lines.

Analog Mux Signals: 3 lines are used to control the enable pins on the 3 BEB muxes, and 3 lines are used to address the mux that is enabled. With polarity as measured on the backplane, a high signal (5V) on the enable pin selects a Mux, and the address pins are reverse logic (111 would select address 0 on the BEB). This allows the implementation of a single AC14 inverting buffer on the BEB for each signal.

AC Test Signal: 2 lines used to provide a test signal to the sensors pre deploy. The signal frequency is settable from 128Hz to 512 kHz and is a square wave. It is activated/deactivated on the 1Hz clock boundary to aid in timing tests during I&T. The AC test line is high on the backplane when disabled, so that the BEB drives low to the boom units after the BEB board inverter.

DAC Control: 4 lines to control the BEB AD5544 Quad DACs. The BEB_DAC_CLK frequency is 1.048 MHz (20^{20}Hz) and is active only on during the transmission of DAC settings. The DACs are serially ganged together. The data is clocked in on the BEB board on the falling edge of BEB_DAC_CLK, polarity as measured on the backplane. The command to the DAC has a 2 bit address followed by 16 bits of data (MSB first). The DACs are serially connected together requiring careful sequencing of the commands in order to ensure correct programming. Data is latched into the DAC registers using the CS pin. Data is latched into the registers on the falling edge of the CS pin as measured on the backplane. Once all the DACs have been loaded consecutively the BEB_DAC_LDAC line is pulsed high. The DACs update on the falling edge of this pulse, polarity as measured on the backplane. Further details can be found in the BEB specification (RBSP_EFW_BEB_001); the interface is shown in figure 5 below.

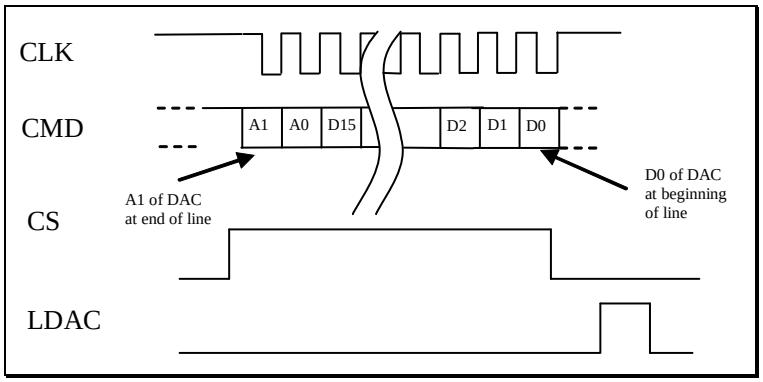


Figure 5 – BEB DAC timing

3.4 LVPS/PCB – DCB Interface

The LVPS/PCB-DCB interface is all 5V logic.

3.4.1 Commands

The LVPS/PCB board receives commands on a three line interface – command (PCB_CMD), clock (PCB_CLK) and strobe (PCB_STB). Commands are 8 bits long, and should be clocked in on the PCB circuit on the falling edge of the PCB_CLK signal (polarity as measured on the backplane). The strobe line PCB_STB is pulsed high after serial transmission of the command (polarity as measured on the backplane). The data is latched in on the PCB on the falling edge of the strobe (polarity as measured on the backplane). The frequency of the PCB_CLK is 1.048 MHz (20^{20}Hz), but the clock is only active for the duration of the command (8 clock cycles per command), the length of the strobe pulse is one full period of PCB_CLK (i.e. 1000ns). The minimum time between commands is 9us, i.e. the next command can follow immediately after the completion of the strobe pulse of the last command, although in practice it is likely to be longer than this. Details of the commands can be found in the LVPS/PCB specification document (RBSP_EFW_LVPS_001). Figure 6 shows the command timing.

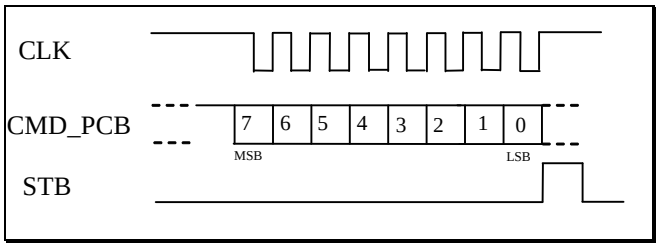


Figure 6 - PCB command timing.

3.4.2 LVPS Converter Clock

The LVPS requires a 799 kHz square wave signal to run the DC-DC converters. This is a 5V signal that will always run, on the event of the DCB failure, the LVPS will free run without this synch signal.

4 Analog Housekeeping

The LVPS/PCB board multiplexes analog housekeeping signals down the backplane on a trace. This is set by command from the DCB using the interface outlined above; command listing for the PCB is contained in the LVPS specification document (RBSP_EFW_LVPS_001). The BEB board also multiplexes analog housekeeping signals down the backplane on a separate trace. More details of the multiplexed signals can be found in the BEB specification (RBSP_EFW_BEB_001). Both signals should be referenced to analog ground.

5 Power Interface

All power to the IDPU boards is provided by the LVPS. This is distributed on the backplane. There are no switched power services on the backplane, i.e. they are always on. There is no power conditioning on the backplane and traces will be made as wide as possible to reduce voltage drop.

6 Physical Interface

The IDPU is housed in a 6U VME wide chassis with a single backplane connecting all the boards together. The board is custom sized to fit into the IDPU chassis. The design is similar to the THEMIS backplane, although the board spacing and number of connectors are different. The ordering of the boards inside the IDPU is: LVPS/PCB on the bottom, the DCB above this, the DFB next followed by the BEB (the most sensitive board to noise) on the top. The backplane board contains traces sandwiched between ground planes. Traces carrying digital signals will be sandwiched between digital ground planes, and the traces carrying analog signals will be sandwiched between analog ground planes. There is no connection between digital and analog ground on the backplane board. Power should be carried on heavy 15 mil wide traces. All remaining pins shall be bussed individually as per the schematic. The backplane board is completely passive. It should be noted that the Backplane pinout differs from the VME standard and boards cannot be used with a standard VME backplane. The part number for the LVPS/PCB connector is an 80 contact pin Hypertronics KA80 1/127CEFD21TABH and the other connectors are all KA98/127CPFD21TABH.

The Hypertronics connectors have a keying mechanism built into the guide posts. They should be set in the following manner:

DCB A & 1
DFB B & 2
BEB C & 3

The pin out for the backplane is listed below in Table 1, connections are shown on the columns on the right, S is send, R is receive. The pin out is also diagrammatically shown in figure 7 below. Spare pins should be connected to all connectors on the backplane. In addition to this;

- DIG_SPARE 7, 8, 9, 11 are jumpered on the DCB to IDPU_DGND.
- ANA_SPARE1,2,3 are jumpered on the DCB to IDPU_AGND

See RBSP_EFW_BPL_003 for schematic.

LVPSPin #	BKP Pin #	Signal Name	Signal Function	LVPS/PCB	DCB	DFB	BEB
	1	DFB_CMD	DFB Command		S	R	R TO GND
	2	DFB_CLK	DFB Clock		S	R	R TO GND
	3	DFB_TLM0	DFB Telemetry Line0		R	S	R TO GND
	4	DFB_CMD	DFB Command		S	R	R TO GND
	5	DFB_1HZ	DFB 1Hz		S	R	R TO GND
	6	DFB_TLM1	DFB Telemetry Line1		R	S	R TO GND
79		LVPS_SPARE1	Spare				
80		LVPS_SPARE2	Spare				
76		LVPS_SPARE3	Spare				
77		LVPS_SPARE4	Spare				
78		LVPS_SPARE5	Spare				
	7	DFB_CLK	DFB Clock		S	R	R TO GND
	8	DFB_1HZ	DFB 1Hz		S	R	R TO GND
73		LVPS_SPARE6	Spare				
75	9	DIG_SPARE9	Spare				
67	10	PCB_CMD	PCB Command	R	S	R TO GND	R TO GND
74	11	DIG_SPARE11	Spare				
	12	BEB_ACTEST2	BEB Actest Line2		S	R TO GND	R
70	13	DIG_SPARE7	Spare				
71	14	DIG_SPARE8	Spare				
72		LVPS_SPARE7	Spare				
	15	BEB_ACTEST1	BEB Actest Line1		S	R TO GND	R
	16	BEB_AMUX_EN0	BEB Analog Mux Enable0		S	R TO GND	R
	17	BEB_AMUX_EN1	BEB Analog Mux Enable1		S	R TO GND	R
	18	BEB_AMUX_EN2	BEB Analog Mux Enable2		S	R TO GND	R
	19	BEB_AMUX_A0	BEB Analog Mux Address0		S	R TO GND	R
	20	BEB_AMUX_A1	BEB Analog Mux Address1		S	R TO GND	R
	21	BEB_AMUX_A2	BEB Analog Mux Address2		S	R TO GND	R
	22	BEB_DAC_CMD	BEB DAC Command		S	R TO GND	R
	23	BEB_DAC_CLK	BEB DAC Clock		S	R TO GND	R
	24	BEB_DAC_LDAC	BEB DAC Load DAC		S	R TO GND	R
	25	BEB_DAC_CS	BEB DAC Chip Select		S	R TO GND	R
68	26	PCB_CLK	PCB Clock	R	S	R TO GND	R TO GND
69	27	PCB_STB	PCB Strobe	R	S	R TO GND	R TO GND
67	28	PCB_CMD	PCB Command	R	S	R TO GND	R TO GND
68	29	PCB_CLK	PCB Clock	R	S	R TO GND	R TO GND
69	30	PCB_STB	PCB Strobe	R	S	R TO GND	R TO GND
64	31	BEB_P5VD	BEB +5VD	S	IDPU_P5VD	IDPU_P5VD	R
65	32	LVPS_CLOCK	LVPS Converter Clock	R	S	R TO GND	R TO GND
66	33	BEB_DGND	BEB Digital Ground	S			R
61	34	IDPU_P5VD	DCB & DFB +5VD	S	R	R	BEB_P5VD
62	35	IDPU_P3.6VD	DCB & DFB +3.6VD	S	R	R	
63	36	IDPU_P1.8VD	DCB & DFB +1.8VD	S	R	R	
58	37	IDPU_DGND	DCB & DFB Digital Ground	S	R	R	BEB_DGND
59	38	IDPU_DGND	DCB & DFB Digital Ground	S	R	R	
60	39	IDPU_DGND	DCB & DFB Digital Ground	S	R	R	
55	40	IDPU_P5VA	IDPU_P5VA	S	R	R	
56	41	IDPU_P3.6VD	IDPU_P3.6VD	S	R	R	

57	42	IDPU_P1.8VD	IDPU_P1.8VD	S	R	R	
52	43	BEB_AGND	BEB Analog Ground	S	ANA_SPARE1	ANA_SPARE 1	R
53	44	BEB_AGND	BEB Analog Ground	S	ANA_SPARE2	ANA_SPARE 2	R
54	45	IDPU_AGND	DCB & DFB Analog Ground	S	R	R	
49	46	BEB_P10VA	BEB +10VA	S	IDPU_P10VA	IDPU_P10VA	R
50	47	BEB_N10VA	BEB -10VA	S	IDPU_N10VA	IDPU_N10VA	R
51	48	IDPU_AGND	DCB & DFB Analog Ground	S	R	R	
46	49	IDPU_P10VA	DCB & DFB +10VA	S	R	R	BEB_P10VA
47	50	IDPU_N10VA	DCB & DFB -10VA	S	R	R	BEB_N10VA
48	51	BEB_ANALOG_HKP	BEB Analog HK		R		S
43	52	IDPU_P5VA	DCB & DFB +5VA	S	R	R	R TO GND
44	53	IDPU_N5VA	DCB & DFB -5VA	S	R	R	R TO GND
45	54	PCB_ANALOG_HKP	PCB Analog HK	S	R		R TO GND
40	55	HV_SPARE20	Spare				BEB_P225V
41	56	IDPU_N5VA	IDPU -5VA	S	R	R	R TO GND
42	57	HV_SPARE22	Spare				BEB_N225V
37	58	BEB_P225V	BEB +225V	S			R
38	59	HV_SPARE19	Spare				
39	60	BEB_N225V	BEB -225V	S			R
34	61	HV_SPARE16	Spare	S			
35	62	HV_SPARE17	Spare				
36	63	HV_SPARE18	Spare	S			
31	64	FV1_P15VA	Floating Voltage +15V	S			R
32	65	FV1_N15VA	Floating Voltage -15V	S			R
33	66	FV1_GND	Floating Voltage GND	S			R
28	67	HV_SPARE13	Spare				
29	68	HV_SPARE14	Spare				
30	69	HV_SPARE15	Spare				
25	70	FV2_P15VA	Floating Voltage +15V	S			R
26	71	FV2_N15VA	Floating Voltage -15V	S			R
27	72	FV2_GND	Floating Voltage GND	S			R
22	73	HV_SPARE10	Spare				
23	74	HV_SPARE11	Spare				
24	75	HV_SPARE12	Spare				
19	76	FV3_P15VA	Floating Voltage +15V	S			R
20	77	FV3_N15VA	Floating Voltage -15V	S			R
21	78	FV3_GND	Floating Voltage GND	S			R
16	79	HV_SPARE7	Spare				
17	80	HV_SPARE8	Spare				
18	81	HV_SPARE9	Spare				
13	82	FV4_P15VA	Floating Voltage +15V	S			R
14	83	FV4_N15VA	Floating Voltage -15V	S			R
15	84	FV4_GND	Floating Voltage GND	S			R
10	85	HV_SPARE4	Spare				
11	86	HV_SPARE5	Spare				
12	87	HV_SPARE6	Spare				
7	88	FV5_P15VA	Floating Voltage +15V	S			R
8	89	FV5_N15VA	Floating Voltage -15V	S			R
9	90	FV5_GND	Floating Voltage GND	S			R
4	91	HV_SPARE1	Spare				
5	92	HV_SPARE2	Spare				
6	93	HV_SPARE3	Spare				
1	94	FV6_P15VA	Floating Voltage +15V	S			R
2	95	FV6_N15VA	Floating Voltage -15V	S			R
3	96	FV6_GND	Floating Voltage GND	S			R

	97	HV_SPARE23	Spare				R TO GND
	98	HV_SPARE24	Spare				R TO GND

Table 1 - Backplane pin out